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(54) Abstract Title
A circuitised substrate for high-frequency applications

(57) A chip carrier (120), or an equivalent circuitised substrate, for high-frequency applications with a multi-layer structure, has via-holes (145) which extend between two non-adjacent conductive layers (210a,210f) for transmitting high-frequency signals. The chip carrier includes, for each via-hole, shielding rings (230b-230e) connectable to a reference voltage; each ring is formed in a corresponding intermediate conductive layer (210b-210e) between the two non-adjacent conductive layers, and is closed around the via-hole. The rings define a shielding coaxial structure for the via-hole. Preferably, the intermediate conductive layers are spaced apart from the via-hole, and particularly from respective lands (125,150), in order to reduce the capacitance of stray capacitors associated with the via-hole (without losing the shielding effect provided by the rings).

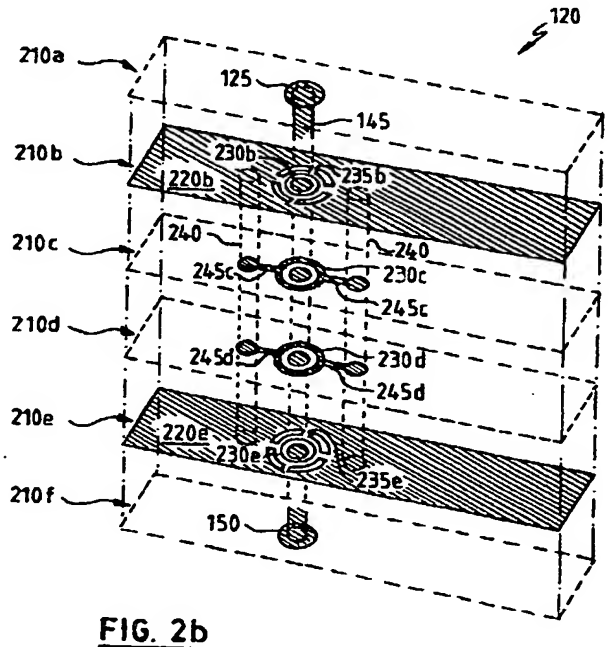

FIG. 2b

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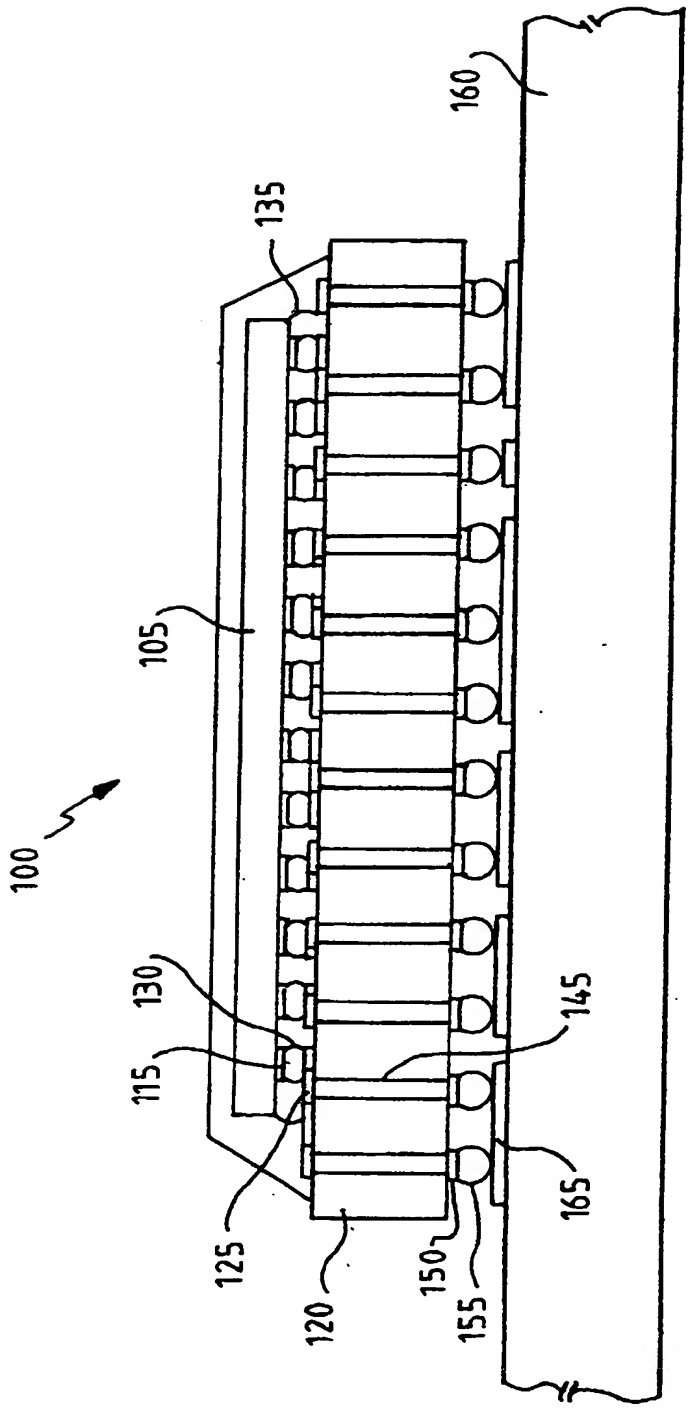


FIG. 1

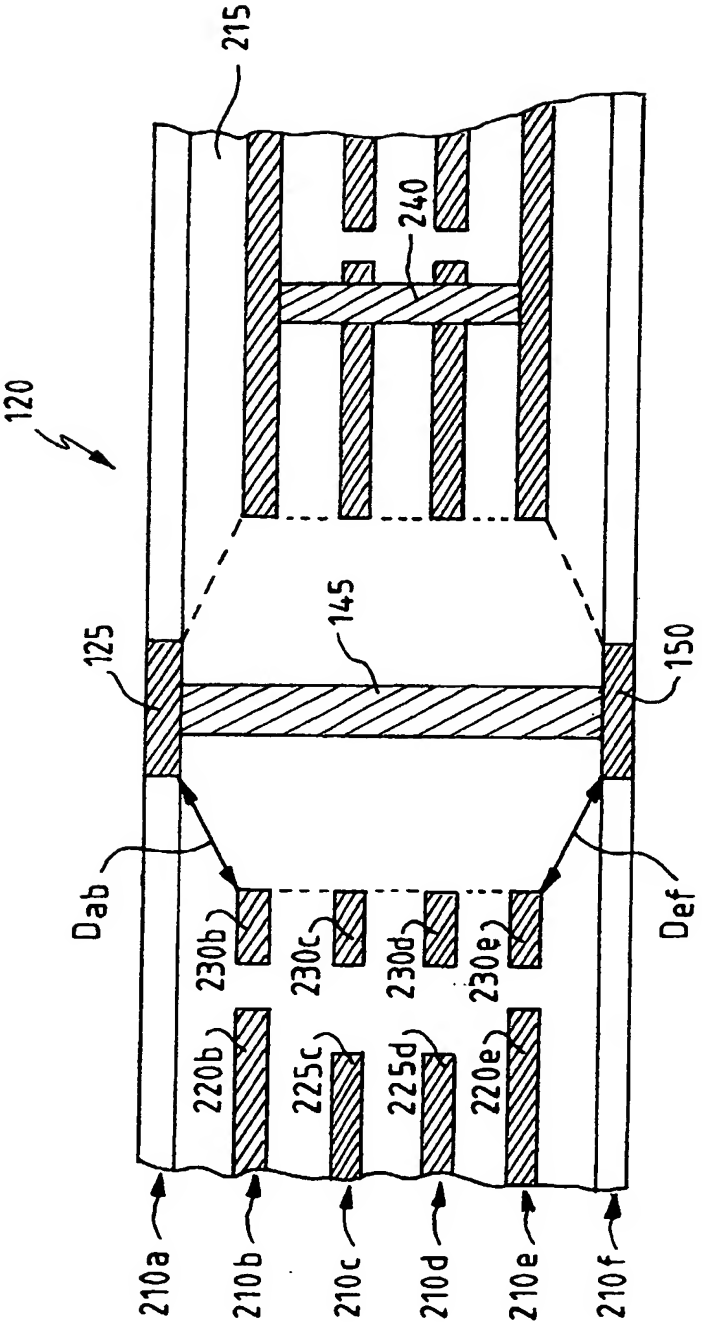

215
240
120
125
145
150
Dab
Def
230b
230c
230d
230e
220b
225c
225d
220e
210a
210b
210c
210d
210e
210f

FIG. 2a

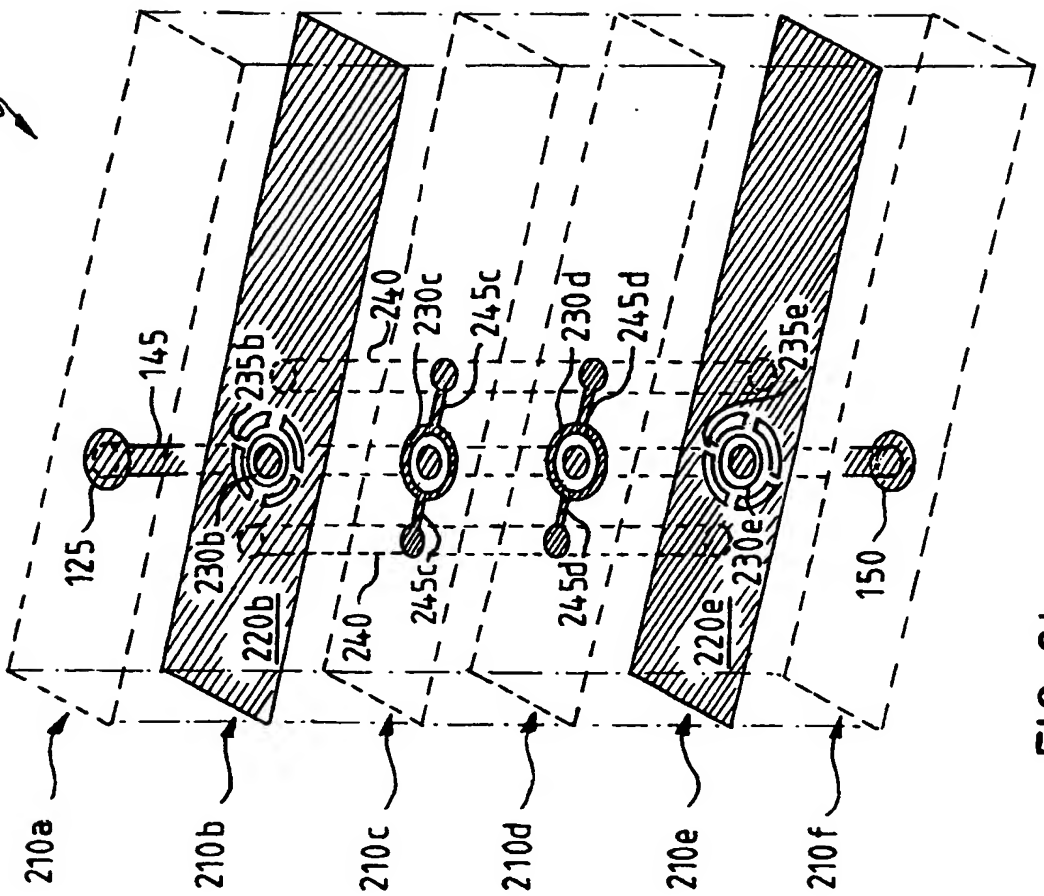

120
145
125
235b
230b
220b
240
230c
245c
240
245c
230d
245d
245d
235e
230e
220e
150
210a
210b
210c
210d
210e
210f

FIG. 2b

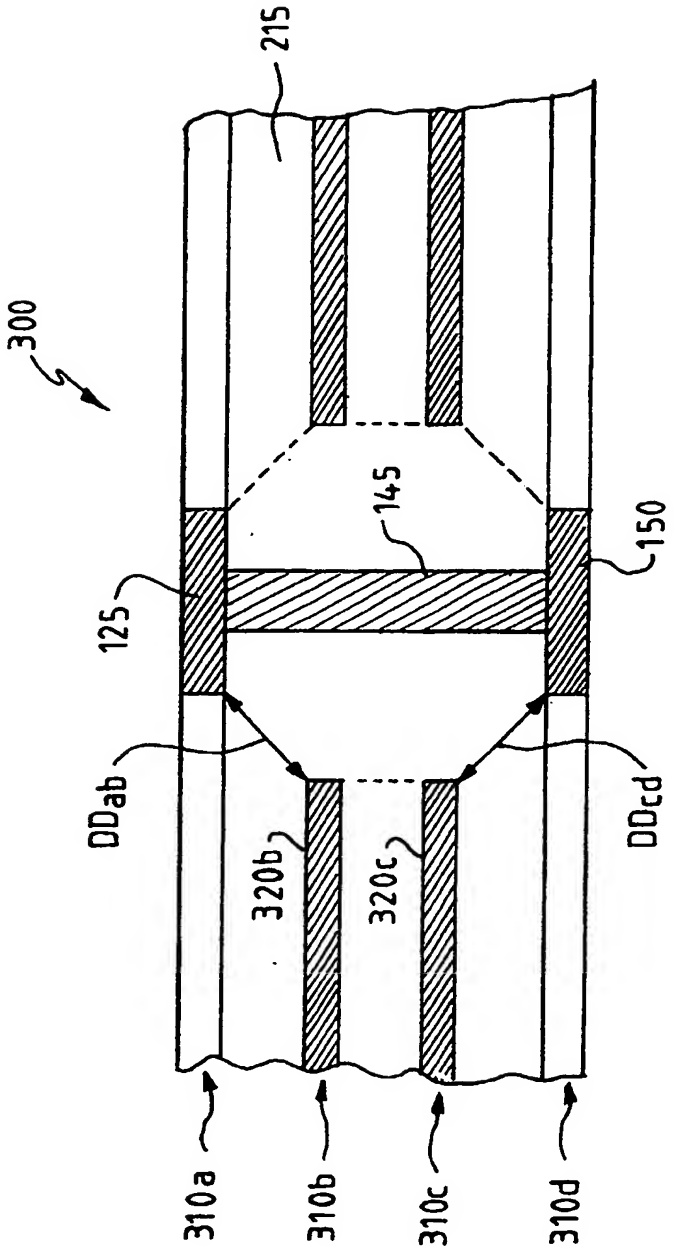


FIG. 3

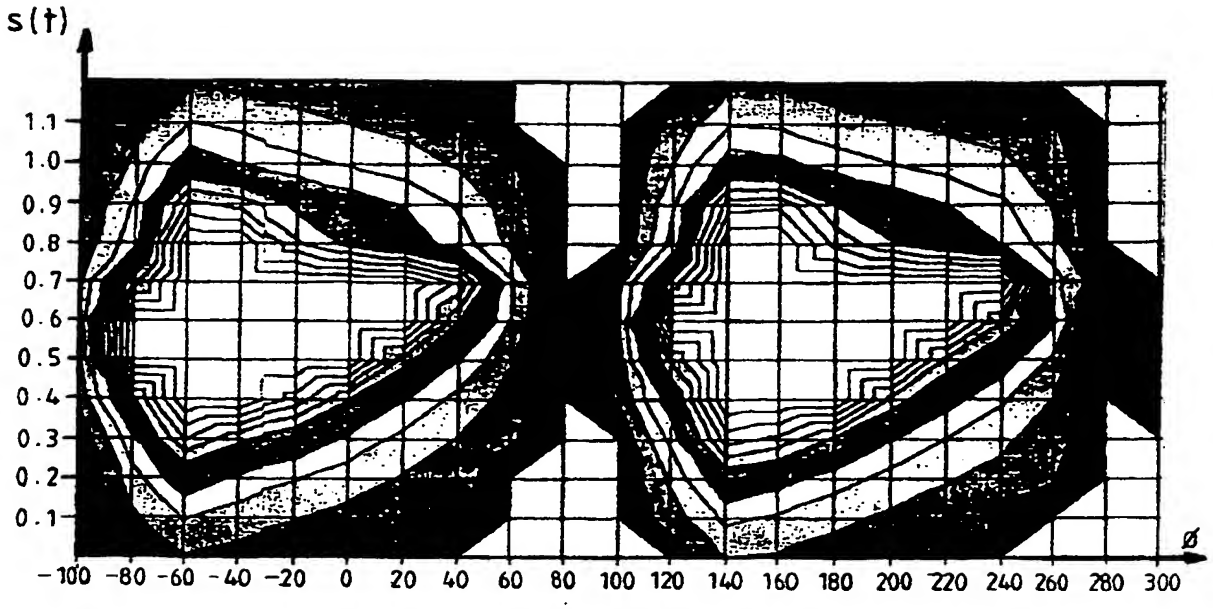
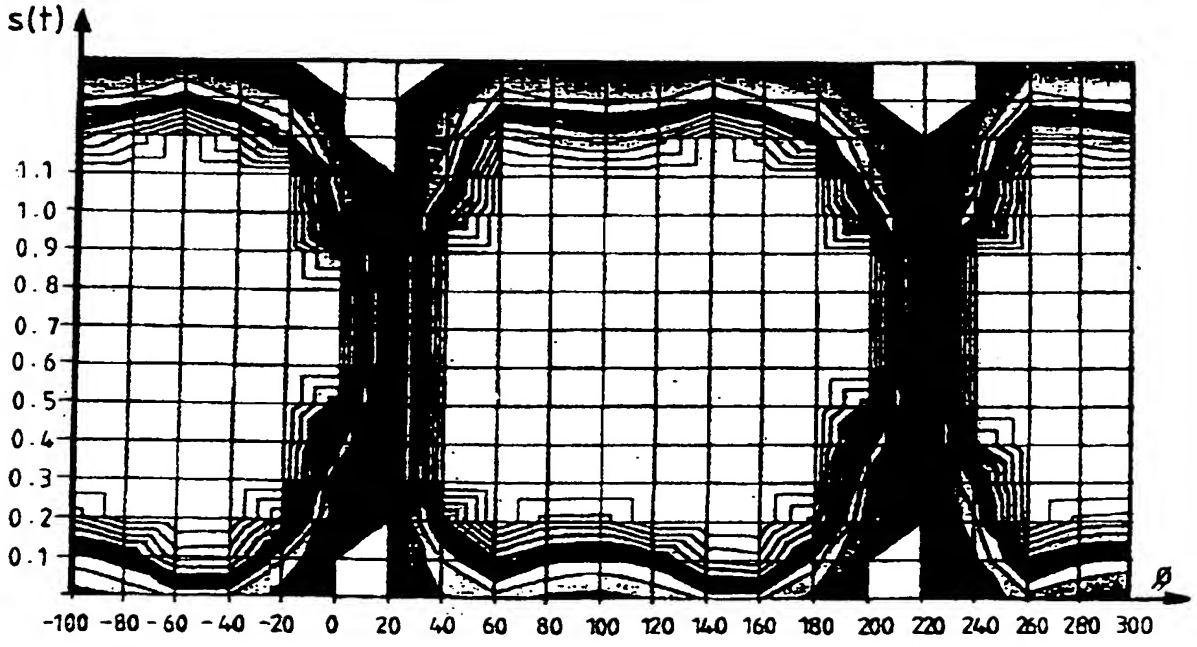

s(t)
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
-100 -80 -60 -40 -20 0 20 40 60 80 100 120 140 160 180 200 220 240 260 280 300
ø

FIG. 4a


s(t)
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1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
-100 -80 -60 -40 -20 0 20 40 60 80 100 120 140 160 180 200 220 240 260 280 300
ø

FIG. 4b

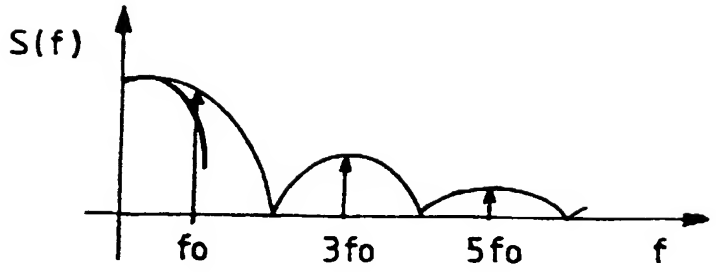

FIG. 5a

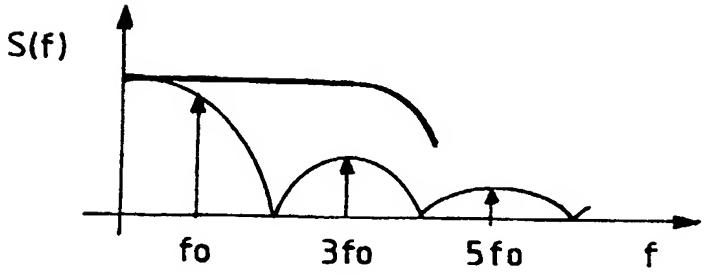

FIG. 5b

A CIRCUITISED SUBSTRATE FOR HIGH-FREQUENCY APPLICATIONS

The present invention relates to a circuitised substrate for high-frequency applications.

Circuitised substrates, consisting of an insulating material provided with conductive tracks defining an electric circuit, are commonly used in several electronic assemblies. For example, the circuitised substrate is employed as a chip carrier for protecting an electronic circuit integrated in a chip of semiconductor material from mechanical stresses. Moreover, the circuitised substrate is also employed as a Printed Circuit Board (PCB) for mounting multiple electronic modules and components.

In some applications, the circuitised substrate has a multi-layer structure, with a plurality of conductive layers insulated from each other; via-holes are used to connect the conductive layers electrically when necessary. The transmission of an electric signal on the corresponding tracks and via-holes generates an electromagnetic wave; the wave propagates along a transmission line defined by a dielectric material surrounding the tracks and the via-holes. When the electronic assembly embedding the circuitised substrate works at a high frequency (for example higher than 1 GHz), the propagation of this wave (microwave) is severely affected by the performance of the electronic assembly as a whole.

Particularly, any discontinuity (or transition) in the transmission line, such as any change in structure, material properties and design features, generates a reflected wave. Moreover, the electronic assembly includes stray structures (capacitors, inductors and resistors), which as a whole act like low pass filters for the transmitted signal. As a consequence, the integrity of the electromagnetic wave propagated along the transmission line is not preserved. For example, a signal switching between a low voltage (logic value 0) and a high voltage (logic value 1) is generated as a square-shaped wave by a driver unit; because of the discontinuities and stray structures associated with the transmission line, the signal is generally received as a pseudo-sinusoidal wave by a different unit.

The quality of the transmission can be visualised by a so-called "eye diagram", which plots the value of the received signal as a function of the phase of a clock signal controlling the switching of the transmitted signal. The above described discontinuities and stray structures associated

with the transmission line reduce the opening of the eye diagram; therefore, it is quite difficult to understand if a switching transition has actually taken place or if the shift of a signal baseline is due to a background noise. Moreover, the received signal features a slow ramp for each switching transition of the transmitted signal. It is then possible that the received signal remains at a stable value for a brief time, even shorter than a settling time needed for recognising the switching transition. As a consequence, the switching transition may not be correctly discriminated from a sudden noise pulse (spike).

These drawbacks are particular acute in modern electronic assemblies working with a reduced level of a power supply voltage (down to 1.2 V). In this case, there is a very low margin to discriminate between the logic value 0 (0V) and the logic value 1 (1.2V).

Therefore, the low quality of the transmission forces the electronic assembly to operate at a frequency far lower than the working frequency that is affordable by an active component of the electronic assembly (such as the electronic circuit integrated in the chip).

It is an object of the present invention to overcome the above-mentioned drawbacks. In order to achieve this object, a circuitised substrate for high-frequency applications as set out in claims 1 and 13 is proposed.

Briefly, the present invention provides a circutised substrate for high-frequency applications including a plurality of conductive layers insulated from each other and at least one via-hole extending between two non-adjacent conductive layers for transmitting a high-frequency signal, at least one intermediate conductive layer being interposed between the two non-adjacent conductive layers; the circuitised substrate further includes, for each via-hole, at least one shielding track connectable to a reference voltage, each shielding track being formed in a corresponding intermediate conductive layer and substantially surrounding the via-hole.

Alternatively, the present invention provides a circutised substrate for high-frequency applications including a plurality of conductive layers insulated from each other, at least one via-hole for transmitting a high-frequency signal, the via-hole extending from a first conductive layer provided on a main surface of the circuitised substrate and ending with a contact area formed in the first conductive layer, and a shielding

structure for the first conductive layer connectable to a reference voltage and formed in a second conductive layer adjacent to the first conductive layer; the shielding structure is arranged outside the contact area in plan view, a distance between the shielding structure and the contact area being inversely proportional to a wavelength of the high-frequency signal according to a factor having a value from $1 \cdot 10^{-6}$ to $10 \cdot 10^{-6}$.

Moreover, the present invention also provides electronic modules for high-frequency applications including these circuitised substrates.

Further features and the advantages of the solution according to the present invention will be made clear by the following description of a preferred embodiment thereof, given purely by way of a non-restrictive indication, with reference to the attached figures, in which:

Fig.1 is a schematic cross-section of an electronic module in which the circuitised substrate of the invention can be used;

Fig.2a and 2b depict a particular of the circuitised substrate and an exploded three-dimensional representation thereof, respectively;

Fig.3 is a cross-section of a different embodiment of the invention;

Fig.4a and 4b show an eye-diagram of a signal in a known electronic module and in the electronic module including the circuitised substrate of the invention, respectively;

Fig.5a and 5b depict the same signals in the frequency domain.

With reference in particular to Fig.1, there is shown an electronic module 100 of the CSP (Chip Scale Package) type. The electronic module 100 includes a chip 105 of semiconductor material, wherein a power circuit working at a high frequency (for example with a clock rate of 10 GHz) is integrated; the chip 105 is supplied by a low voltage power supply (for example of 1.2V relative to a reference voltage, or ground). Several contact terminals 115 (for example some tens) are formed through a dielectric layer that protects an active surface of the chip 105.

The chip 105 is mounted on a carrier 120 consisting of an insulating circuitised substrate. The mounting is made with a flip-chip technique, wherein the active surface of the chip 105 (including the contact terminals

115) faces an upper surface of the chip carrier 120. Particularly, contact pads 125 corresponding to the contact terminals 115 are formed through a solder mask that protects the upper surface of the chip carrier 120. The contact terminals 115 are soldered to the contact pads 125 by means of respective bumps 130, which connect the chip 105 to the carrier 120 mechanically and electrically.

An under-filling material 135 (such as an epoxy resin) is interposed between the chip 105 and the carrier 120; the under-filling material 135 improves the mechanical connection between the chip 105 and the carrier 120 (compensating for their different coefficients of thermal expansion), and protects the chip 105 and the electrical connections with the chip carrier 120 from the external environment.

The contact pads 125 are connected to plated through holes (or via-holes) 145, either by means of conductive tracks formed on the upper surface of the chip carrier 120 or directly (in this case, the contact pads 125 are generally referred to as lands). The via-holes 145 are in turn connected to further lands 150 formed on a lower surface of the chip carrier 120. Interconnecting balls 155 (made of a eutectic solder, such as a Tin Lead alloy) are grown on the respective lands 150.

The electronic module 100 is typically mounted on a printed circuit board 160 by soldering the interconnecting balls 155 onto corresponding conductive tracks 165. Typically, multiple electronic modules and components (such as discrete resistors and capacitors) are mounted on the printed circuit board 160; the assembly formed by the printed circuit board 160 and the electronic modules and components mounted thereon is commonly referred to as an electronic board.

Likewise considerations apply if the electronic module has a different structure, for example if it is of the BGA (Ball Grid Array) type, wherein the chip is mounted on the carrier with the active surface turned upward and it is wire-bonded thereto, if the chip does not embody a (digital) power circuit, if it works at a different frequency or with a different power supply, and so on.

Considering now Fig.2a, the chip carrier 120 has a multi-layer structure, with several conductive layers insulated from each other. In the example at issue, the chip carrier 120 includes six conductive layers 210a, 210b, 210c, 210d, 210e and 210f (made for example of copper), which are

insulated from each other by means of a dielectric material 215 (made for example of an epoxy resin with glass fibres); typically, a dielectric layer arranged between each couple of adjacent conductive layers 210a-210f has a thickness of 110μm.

The land 125 is formed in the first conductive layer 210a (starting from the upper surface of the chip carrier 120), while the land 150 is formed in the last conductive layer 210f. The land 125, the via-hole 145 and the land 150 are used to transmit a high-frequency signal between the chip (on the upper surface of the chip carrier 120) and the printed circuit board (on the lower surface of the chip carrier 120).

A ground plane 220b is formed in the second conductive layer 210b (adjacent to the first conductive layer 210a), and a further ground plane 220e is formed in the last but one conductive layer 210e (adjacent to the last conductive layer 210f). The ground planes 220b and 220e feature a couple of coaxial openings for each via-hole 145. One or more further via-holes (not shown in the figure) are used to connect the ground planes 220b and 220e to the reference voltage. Multiple signal tracks 225c and 225d are formed in the conductive layers 210c and 210d, respectively.

The high-frequency signal transmitted between the chip and the printed circuit board generates an electromagnetic wave. The electromagnetic wave propagates along a transmission line defined by the elements 125,145,155 and a reference structure formed by the ground planes 220b,220e; the ground planes 220b,220e control an impedance of the transmission line (typically tailored to a value of 50Ω) and shield the same from electromagnetic interference.

The inventors have discovered that the degradation in the performance of the known electronic modules is mainly due to a discontinuity of the transmission line associated with the via-hole 145. Moreover, the via-hole 145 generates stray capacitors that have a relative high capacitance (of the order of 500fF). Particularly, stray capacitors are formed between the land 125 and the underlying ground plane 220b, and between the land 150 and the underlying ground plane 220e; further stray capacitors are formed by the coupling of the via-hole 145 with the intermediate (inner) conductive layers 210b-210e interposed between the conductive layers 210a and 210f.

In a preferred embodiment of the present invention, as shown in the exploded three-dimensional representation of Fig.2b, the inner conductive

layers 210b, 210c, 210d and 210e include a shielding ring 230b, 230c, 230d and 230e, respectively; each ring 230b-230e is formed by a circular track (for example with a width of 100μm), which is closed around the via-hole 145. Particularly, the via-hole 145 is arranged at a centre of each ring 230b-230e (without interposition of any other conductive element). The rings 230b,230e are obtained removing four arc-shaped portions of the ground planes 220b,220e; in this way, the rings 230b,230e are connected to a remaining portion of the ground planes 220b,220e through four radial conductive segments 235b,235e. Two via-holes 240 (opposed to the via-hole 145) extend between the ground planes 220b and 220e. Conductive segments 245c and 245d connect the rings 230c and 230d, respectively, to the via-holes 240 (and then to the reference voltage).

Referring back to Fig.2a, the rings 230b-230e are arranged outside the lands 125,155 in plan view. Particularly, a distance Dab between an internal border of the ring 230b and an outline of the land 125 and a distance Def between an internal border of the ring 230e and an outline of the land 150 are inversely proportional to a wavelength λ of the signal transmitted along the elements 125,145,150 according to a factor having a value from $1 \cdot 10^{-6}$ and $10 \cdot 10^{-6}$; preferably, the factor has a value from $4 \cdot 10^{-6}$ to $5 \cdot 10^{-6}$, such as $4.2 \cdot 10^{-6}$. In the example at issue, wherein the signal has a frequency f=10GHz (assuming that the dielectric material has a dielectric constant ε_r=3.75 and a diamagnetic constant μ=1), the distance Dab,Def is:

$$Dab, Def = \frac{4.2 \cdot 10^{-6}}{\lambda} = \frac{4.2 \cdot 10^{-6} \cdot f \cdot \sqrt{\varepsilon_r \cdot \mu}}{c} = \frac{4.2 \cdot 10^{-6} \cdot 10 \cdot 10^{9} \cdot \sqrt{3.75 \cdot 1}}{2.998 \cdot 10^{8}} = 271 \cdot 10^{-6} = 271 \mu m$$

The other rings 230c-230d are arranged in plan view outside a clearance window defined orthographically projecting the internal border of the rings 230b and 230e on a plane of the corresponding conductive layers 210c-210d.

Likewise considerations apply if the chip carrier has a different structure, for example with couples of differential via-holes, if the chip carrier includes a different number of conductive layers, if the dielectric material has a different thickness, if the ground planes are replaced by equivalent shielding structures (for example consisting of two or more tracks), if couples of coplanar shielding tracks are provided on the upper

surface of the chip carrier, if the rings have a different width, and so on.

More generally, the present invention provides a circutised substrate for high-frequency applications including a plurality of conductive layers insulated from each other and one or more via-holes extending between two non-adjacent conductive layers for transmitting a high-frequency signal; one or more intermediate conductive layers are interposed between the two non-adjacent conductive layers. The circuitised substrate further includes, for each via-hole, one or more shielding tracks connectable to a reference voltage; each shielding track is formed in a corresponding intermediate conductive layer and substantially surrounds the via-hole.

The devised solution provides a mesh shielding of the via-hole, which acts as a coaxial structure.

The solution of the invention optimises the propagation of the electromagnetic wave through the transition associated with the via-hole, and maintains a good integrity of the electromagnetic wave along the transmission line. The proposed design of the circuitised substrate affects the performance of an active component associated therewith (such as the electronic circuit integrated in the chip) as little as possible.

The devised structure does not require any substantial change in the manufacturing process of the circuited substrate, so that these results are achieved at no extra cost.

The preferred embodiment of the invention described above offers further advantages. Particularly, the rings closed around the via-hole provide a complete shielding path; moreover, the arrangement of the via-hole at the centre of the rings ensures that no asymmetry is introduced. Preferably, the rings are formed in each inner conductive layer, so that they are as close as possible to each other (given a pre-set thickness of the dielectric layer arranged between them). This results in a very low pitch of the mesh structure around the via-hole, which provides a good shielding for signals with a very high frequency. Experimental results have shown that the mesh structure achieves a reasonable shielding of signals with a wavelength λ_{max} up to four times the pitch of the mesh structure. In the example at issue, wherein the dielectric layer has a thickness of 110μm (with a dielectric constant ε_r=3.75 and a diamagnetic constant μ=1), the mesh structure is effective to shield signals with a frequency f_{max} up to:

$$f_{max} = \frac{c}{\lambda_{max} \cdot \sqrt{\varepsilon_r \cdot \mu}} = \frac{2.998 \cdot 10^8}{4 \cdot 110 \cdot 10^{-6} \cdot \sqrt{3.75 \cdot 1}} = 352 \cdot 10^9 = 352GHz$$

Alternatively, the rings are not completely closed around the via-hole, the rings are replaced by square frames or by generic tracks substantially surrounding the via-hole, the rings are not formed in all the inner conductive layers (for example with a ring every two or more conductive layers).

The solution of the invention is particularly advantageous when the via-hole is a plated though hole extending between the first and the last conductive layer (with multiple inner layers arranged between them). Moreover, the particular solution devised for connecting the rings to the reference voltage (with the conductive segments for reaching the remaining part of the ground planes or the further via-holes extending between the ground planes) is particularly effective and does not interfere with the shielding provided by the mesh. Preferably, the further via-holes are symmetrically arranged around the via-hole, in order to keep the structure as balanced as possible.

However, the solution of the invention leads itself to be implemented even in a circuitised substrate with a reduced number of conductive layers (down to three), with via-holes extending between inner layers, with a different number of conductive segments for each ring, with a different number of further via-holes (down to a single one), with the rings connected to the reference voltage in a different manner.

The rings spaced apart from the via-hole (and particularly from the respective lands) strongly reduce the capacitance of the stray capacitor formed between the lands and the ground planes and between the via-hole and the inner conductive layers (being inversely proportional to their distance); in the example at issue, the arrangement of the rings outside the lands in plan view reduces the capacitance of the aforementioned capacitors down to 10-20fF. Moreover, experimental results have shown that the values proposed for the distance between the rings and the lands provide the best performance of the electronic module; the arrangement of the inner conductive layers outside the clearance window further improves the performance of the electronic module at high frequency. As a matter of fact, the proposed structure ensures a good reduction of the stray capacitances, without loosing the shielding effect provided by the rings.

It should be noted that this result is obtained with a negligible wastage of area on the chip carrier, since only few via-holes are typically used for transmitting high-frequency signals (for example less than 10% of all the via-holes included in the chip carrier).

Similar considerations apply if the distance between the rings and the lands are determined differently, or if the clearance window is defined in a different manner. Alternatively, the rings are arranged in another position; for example, only the rings formed in the second and in the last but one conductive layer are spaced apart from the via-hole, the inner borders of the rings are vertically aligned with the outline of the lands, or the rings are inside the lands in plan view.

Preferably, the circuitised substrate of the invention is used as a carrier for a circuit integrated in a chip of semiconductor material. The advantageous effects provided by the envisaged solution greatly improve the performance of the corresponding electronic module; particularly, this allows the electronic module to be operated at a frequency very close to the working frequency which is afforded by the chip.

However, the circuitised substrate according to the present invention leads itself to be used even as a PCB in an electronic board, or in other electronic assemblies.

It should be noted that the additional features relating to the particular arrangement of the inner conductive layers around the via-hole are suitable to be used (alone or in combination with the other additional features) even without the shielding rings described above.

With reference in particular to Fig.3 (the elements corresponding to the ones shown in the Fig.2a are denoted with the same references, and their explanation is omitted for the sake of simplicity), there is shown a chip carrier 300 (corresponding to the chip carrier 120 of Fig.1) according to an alternative embodiment of the invention. The chip carrier 300 includes four conductive layers 310a, 310b, 310c and 310d, which are insulated from each other by means of the dielectric material 215. The land 125 is formed in the first conductive layer 310a (starting from the upper surface of the chip carrier 300), while the land 150 is formed in the last conductive layer 310d.

A ground plane 320b is formed in the second conductive layer 310b (adjacent to the first conductive layer 310a), and a power plane 320c is formed in the last but one conductive layer 310c (adjacent to the last conductive layer 310d). The ground plane 320b and the power plane 320c feature a couple of coaxial openings for each via-hole 145. One or more further via-holes (not shown in the figure) are used to connect the ground plane 320b and the power plane 320c to the reference voltage and to the power supply voltage, respectively.

The ground plane 320b and the power plane 320c are arranged outside the lands 125,155 in plan view. Particularly, a distance DDab between a border of the ground plane 320b (that is an internal border of the opening for the via-hole 145) and an outline of the land 125 is inversely proportional to a wavelength λ of the signal transmitted along the elements 125,145,150. More specifically, the distance DDab is (inversely) proportional to the wavelength λ according to a factor having a value from $1 \bullet 10^{-6}$ and $10 \bullet 10^{-6}$; preferably, the factor has a value from $4 \bullet 10^{-6}$ to $5 \bullet 10^{-6}$, such as $4.2 \bullet 10^{-6}$. In a similar manner, a distance DDcd between a border of the power plane 320c (that is an internal border of the opening for the via-hole 145) and an outline of the land 150 is inversely proportional to the wavelength λ of the signal according to the same factor.

Likewise considerations apply if the chip carrier has a different structure, if the chip carrier includes a different number of conductive layers (for example with two ground planes and one or more signal tracks arranged between them), if the ground plane and the power plane are replaced by equivalent structures (for example consisting of two or more tracks), if the distance between the ground/power planes and the lands is determined in a different manner, if the proposed arrangement is applied only to one out of the ground plane and the power plane, and so on.

More generally, the present invention further provides a circuitised substrate for high-frequency applications including a plurality of conductive layers insulated from each other. One or more via-holes for transmitting a high-frequency signal extend from a first conductive layer provided on a main surface of the circuitised substrate and end with a contact area formed in the first conductive layer. The insulated substrate further includes a shielding structure for the first conductive layer connectable to a reference voltage and formed in a second conductive layer adjacent to the first conductive layer. The shielding structure is arranged

outside the contact area in plan view; a distance between the shielding structure and the contact area is inversely proportional to a wavelength of the high-frequency signal according to a factor having a value from $1 \bullet 10^{-6}$ to $10 \bullet 10^{-6}$.

The proposed arrangement of the ground/power planes strongly reduces the capacitance of the stray capacitors associated with the via-hole (and particularly with the respective lands). This result is obtained with a solution that is in sharp contrast to the common practise of keeping the ground/power planes (or more generally any reference structure) as close as possible to the via-hole. Conversely, the inventors have discovered that the devised structure provides the best performance of the electronic module, since it ensures a good reduction of the stray capacitances, without loosing the shielding effect provided by the ground/power planes. As explained above, this solution does not affect the dimension of the chip carrier, since only few via-holes are typically used for transmitting high-frequency signals.

Both the embodiments of the present invention strongly improve the performance of the electronic module including the chip carrier. With reference in particular to Fig.4a, there is depicted an eye-diagram for a known electronic module. This diagram shows the value (in V) of a signal s(t) received from a transmission line as a function of the phase (ϕ) of a clock signal; the eye-diagram is quite close, due to the discontinuities and stray capacitors associated with the transmission line.

Conversely, an eye-diagram for the electronic module embedding the chip carrier of the invention, as shown in Fig.4b, is more open, so that it is easier to discriminate an actual switching transition of the signal from a spike or from a shift of a signal baseline due to a background noise. As a consequence, the electronic module can be operated at a high frequency even with a reduced level of the power supply voltage.

In other words, in the known electronic module the low-pass filter defined by the stray capacitors formed between the lands and the ground/power planes and between the inner conductive layers and the via-hole has a very low cut-off frequency; therefore, as shown in Fig.5a, only the first harmonic f0 of the signal s(f) expressed in the frequency domain (f) is hardly transmitted. On the other hand, the solution of the invention increases the bandwidth of the transmission line up to the third harmonic 3f0 of the signal, as shown in Fig.5b.

Naturally, in order to satisfy local and specific requirements, a person skilled in the art may apply to the solution described above many modifications and alterations all of which, however, are included within the scope of protection of the invention as defined by the following claims.

CLAIMS

1. A circutised substrate (120) for high-frequency applications including a plurality of conductive layers (210a-210f) insulated from each other and at least one via-hole (145) extending between two non-adjacent conductive layers (210a,210f) for transmitting a high-frequency signal, at least one intermediate (210b-210e) conductive layer being interposed between the two non-adjacent conductive layers, characterised in that the circuitised substrate further includes, for each via-hole, at least one shielding track (230b-230e) connectable to a reference voltage, each shielding track being formed in a corresponding intermediate conductive layer and substantially surrounding the via-hole.

2. The circuitised substrate (120) according to claim 1, wherein each shielding track includes a ring (230b-230e) closed around the via-hole (145), the via-hole being arranged at a centre of the ring.

3. The circuitised substrate (120) according to claim 1 or 2, wherein the at least one intermediate conductive layer (210b-210e) consists of a plurality of intermediate conductive layers, the shielding track (230b-230e) being formed in each intermediate conductive layer.

4. The circuitised substrate (120) according to any claim from 1 to 3, wherein the two non-adjacent conductive layers (210a,210f) are a first conductive layer (210a) provided on a main surface of the circuitised substrate and a last conductive layer (210f) provided on a further main surface of the circuitised substrate opposed to the main surface.

5. The circuitised substrate (120) according to claim 4, wherein a second conductive layer (210b) adjacent to the first conductive layer (210a) includes a shielding structure (220b) for the first conductive layer connectable to the reference voltage and a last but one conductive layer (210e) adjacent to the last conductive layer (210f) includes a further shielding structure (220e) for the last conductive layer connectable to the reference voltage, the second (210b) and the last but one (220e) conductive layer further including, for each shielding track (230b;235e), at least one conductive segment (235b;235e) connecting the shielding track to the corresponding shielding structure.

6. The circuitised substrate (120) according to claim 5, wherein at least one further via-hole (240) extends between the shielding structure

(220b) and the further shielding structure (220e), each intermediate conductive layer (210c,210d) distinct from the second (210b) and the last but one (210e) conductive layer further including, for each shielding track (230c;230d), at least one conductive segment (245c;245d) connecting the shielding track to the at least one further via-hole.

7. The circuitised substrate (120) according to claim 6, wherein the at least one further via-hole (240) consists of a plurality of further via-holes symmetrically arranged around the via-hole (145).

8. The circuitised substrate (120) according to any claim from 4 to 7, wherein each via-hole (145) ends with a contact area (125) formed in the first conductive layer (210a) and with a further contact area (150) formed in the last conductive layer (210f), each shielding track (230b-230e) being arranged outside the contact area and the further contact area in plan view.

9. The circuitised substrate (120) according to claim 8, wherein a distance between the shielding track (230b) formed in the second conductive layer (210b) and the contact area (125) and a distance between the shielding track (230e) formed in the last but one conductive layer (210e) and the further contact area (150) are inversely proportional to a wavelength of the high-frequency signal according to a factor having a value from $1 \bullet 10^{-6}$ to $10 \bullet 10^{-6}$.

10. The circuitised substrate (120) according to claim 9, wherein said factor has a value from $4 \bullet 10^{-6}$ to $5 \bullet 10^{-6}$.

11. The circuitised substrate (120) according to claim 9 or 10, wherein each intermediate layer (210c,210d) distinct from the second (210b) and the last but one (210e) conductive layer is arranged in plan view outside a clearance window defined orthographically projecting an internal border of the shielding track (230b) formed in the second conductive layer (210b) and an internal border of the shielding track (230e) formed in the last but one conductive layer (210e) on a plane of the intermediate layer.

12. A high-frequency electronic module (100) including a chip of semiconductor material (105) with a plurality of terminals (115), the circuitised substrate (120) according to any claim from 1 to 11, the chip being mounted on the circuitised substrate, and means (130) for

electrically connecting each via-hole (145) of the circuitised substrate to a corresponding terminal of the chip.

13. A circutised substrate (300) for high-frequency applications including a plurality of conductive layers (310a-310d) insulated from each other, at least one via-hole (145) for transmitting a high-frequency signal, the via-hole extending from a first conductive layer (210a) provided on a main surface of the circuitised substrate and ending with a contact area (125) formed in the first conductive layer, and a shielding structure (320b) for the first conductive layer connectable to a reference voltage and formed in a second conductive layer (310b) adjacent to the first conductive layer, characterised in that the shielding structure is arranged outside the contact area in plan view, a distance between the shielding structure (320b) and the contact area (125) being inversely proportional to a wavelength of the high-frequency signal according to a factor having a value from $1 \bullet 10^{-6}$ to $10 \bullet 10^{-6}$.

14. The circuitised substrate (300) according to claim 13, wherein said factor has a value from $4 \bullet 10^{-6}$ to $5 \bullet 10^{-6}$.

15. The circuitised substrate (300) according to claim 13 or 14, further including a supply structure (320c) connectable to a power supply voltage and formed in a last but one conductive layer (310c) adjacent to a last conductive layer (310e) provided on a further main surface of the circuitised substrate opposed to the main surface, the via-hole (145) extending from the first conductive layer (310a) to the last conductive layer (310d) and ending with a further contact area (150) formed in the last conductive layer, wherein a distance between the supply structure (320c) and the further contact area (150) is inversely proportional to the wavelength of the high-frequency signal according to said factor.

16. A high-frequency electronic module (100) including a chip of semiconductor material (105) with a plurality of terminals (115), the circuitised substrate (300) according to any claim from 13 to 15, the chip being mounted on the circuitised substrate, and means (130) for electrically connecting each via-hole (145) of the circuitised substrate to a corresponding terminal of the chip.

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1R (RAL, RAN, RAS, RBH)

Int Cl (Ed.7): H01L, H05K

Other: Online: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0180183 A2	(TOSHIBA)	
A	US 5929375	(GLOVATSKY)	
A	JP 050036859	(MATSUSHITA)	

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